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Our Docket No.: 042390.P5549

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	
Bogin et al.	Examiner: Elmore, R.
Application No.: 09/205,086	Art Group: 2187
Filed: December 4, 1998	
For: Method and Apparatus for Self Timing Refresh	

APPEAL BRIEF
IN SUPPORT OF APPELLANT'S APPEAL
TO THE BOARD OF PATENT APPEALS AND INTERFERENCES

Sir:

Appellant hereby submits this Brief in triplicate in support of its appeal from a final decision by the Examiner, mailed April 18, 2002, in the above-referenced Application. Appellant respectfully requests consideration of this appeal by the Board of Patent Appeals and Interferences for allowance of the above-captioned patent application.

An oral hearing is not desired.

FIRST CLASS CERTIFICATE OF MAILING
(37 C.F.R. § 1.8 (a))

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I. REAL PARTY IN INTEREST

The invention is assigned to Intel Corporation of 2200 Mission College Boulevard, Santa Clara, California 95052.

II. RELATED APPEALS AND INTERFERENCES

To the best of Appellant's knowledge, there are no appeals or interferences related to the present appeal that will directly affect, be directly affected by, or have a bearing on the Board's decision.

III. STATUS OF THE CLAIMS

Claims 1-28 and 38-49 are currently pending in the above-referenced application. Claims 1-28 and 38-49 stand rejected under U.S.C. §102(b) as being anticipated by a Direct Rambus Technology Disclosure ("*The Rambus Disclosure*") in the Final Office Action mailed April 18, 2002.

IV. STATUS OF AMENDMENTS

In response to the Final Office Action mailed on April 18, 2002, rejecting claims 1-28 and 38-49 under 35 U.S.C. §102(b), Appellant filed an Amendment After Final Office Action under 37 C.F.R. § 1.116. Also, Appellant filed a Notice of Appeal on July 10, 2002. A copy of all claims on appeal is attached hereto as an Appendix of Claims.

V. SUMMARY OF THE INVENTION

According to one embodiment, a computer system is described. The computer system includes a memory and a memory controller. The memory controller includes a refresh timing circuit that generates clock pulses used to trigger memory refresh events. In a further embodiment, a memory controller is disclosed. The memory controller includes a refresh timing circuit that generates clock pulses that are used to trigger memory refresh events. Further, a refresh timing circuit is disclosed, the refresh timing circuit includes an internal clock generator, a first counter coupled to the clock generator, a storage register coupled to the clock generator and the counter, and a comparator coupled to the clock generator, the counter and the storage register.

VI. ISSUES PRESENTED

Whether claims 1-28 and 38-49 are patentable over *The Rambus Disclosure* under 35 U.S.C. §102(b).

VII. GROUPING OF CLAIMS

The claims do not stand or fall together.

For the purposes of this appeal:

Claims 1, 2, 15 and 16 stand or fall together as Group I; and

Claims 3-14, 17-27 and 38-49 stand or fall together as Group II.

Reasons for separate patentability of the above indicated Claim Groups I and II are presented in the arguments section pursuant to 37 C.F.R. § 1.192(c)(7).

VIII. ARGUMENT

1. Claim Group I

THE PENDING CLAIMS WERE IMPROPERLY REJECTED UNDER 35 U.S.C. § 102(b) BECAUSE *THE RAMBUS DISCLOSURE* DOES NOT DISCLOSE A MEMORY CONTROLLER COMPRISING A REFRESH TIMING CIRCUIT FOR GENERATING CLOCK PULSES USED TO TRIGGER MEMORY REFRESHES

Appellant respectfully submits that *The Rambus Disclosure* fails to anticipate the claimed invention for the reasons set forth below.

Each claim in Claim Group I recites an element that is not disclosed in *The Rambus Disclosure.* For example, Appellant's claim 1 recites the following:

> A computer system comprising:
> a memory; and
> memory controller, wherein the memory controller includes a refresh timing circuit for generating clock pulses used to trigger memory refresh events.

Appellant's claim 16 recites:

> A memory controller comprising:
> a refresh timing circuit for generating clock pulses used to trigger memory refresh events.

The Rambus Disclosure describes a memory controller that supports refreshes. However, the disclosure of a memory controller with refresh control is not analogous, nor implicit, of a memory controller having a refresh timing circuit for generating clock pulses used to trigger memory refreshes. The Examiner asserts that:

> [T]he Rambus memory controller is a controller for dynamic RAM (DRAM) which inherently requires refreshing in order to maintain coherency of the stored data. On page 14 of the reference it is

> states that the RMC supports all control functions including protocol, refresh memory and interleaving support. In order to support refresh functions clock pulses must be used to trigger memory refreshes necessary for DRAM. It is admitted that there is not a great deal of details given in relationship to refresh functions . . .

(See Final Office Action at page 2, paragraph 4).

Appellant submits, however, that although the RMC may control refreshing using clock function triggers, no timing circuitry is disclosed that generates the clock pulses that trigger the refresh. Moreover, Appellant submits that for anticipation under 35 U.S.C. 102(b), a reference must teach every aspect of the claimed invention either explicitly or inherently. The Examiner admits that *the Rambus Disclosure* does not disclose refresh timing circuitry, and relies upon the RMC inherently disclosing such circuitry.

However, it is not inherent that a memory controller includes refresh timing circuitry. In fact prior art memory controllers, such as the RMC disclosed in *the Rambus Disclosure*, receive clock pulses from an external clock source in order to trigger a memory refresh. See page 3, lines 6-11 of Appellant's Background section. Receiving clock pulses from an external clock source requires an additional pin to be used that may lead to an increase in circuit complexity (page 3, lines 12-19). Therefore, Claim Group I is patentable over *the Rambus Disclosure*.

For the foregoing reasons, Appellant submits that the Examiner has failed to search and find a printed publication or patent that discloses the claimed invention as set forth in MPEP § 706.02(a).

Claims 2 and 15 depend from claim 1. Given that dependent claims necessarily include the limitations of the claims from which they depend, Appellant submits that the invention as claimed in claims 2 and 15 are similarly not anticipated

by *The Rambus Disclosure*.

Thus, the Examiner erred in rejecting claims 1, 2, 15 and 16 under U.S.C. § 102(b).

2. Claim Group II

THE PENDING CLAIMS WERE IMPROPERLY REJECTED UNDER 35 U.S.C. § 102(b) BECAUSE *THE RAMBUS DISCLOSURE* DOES NOT DISCLOSE A REFRESH TIMING CIRCUIT HAVING AN INTERNAL CLOCK GENERATOR, A FIRST COUNTER COUPLED TO THE CLOCK GENERATOR, A STORAGE REGISTER COUPLED TO THE CLOCK GENERATOR AND THE COUNTER, AND A COMPARATOR COUPLED TO THE CLOCK GENERATOR, THE COUNTER AND THE STORAGE REGISTER

Claims 3-14, 17-27, and 38-49 of Claim Group II are not anticipated under 35 U.S.C. §102(b) for the same reasons as given above with respect to Claim Group I and further due to the additional limitation of a refresh timing circuit having an internal clock generator, a first counter coupled to the clock generator, a storage register coupled to the clock generator and the counter, and a comparator coupled to the clock generator, the counter and the storage register.

The claims of Claim Group II are drawn to a refresh timing circuit having an internal clock generator, a first counter coupled to the clock generator, a storage register coupled to the clock generator and the counter, and a comparator coupled to the clock generator, the counter and the storage register. Appellant's arguments made above with respect to the claims of Claim Group I apply equally to Claim Group II and are incorporated herein by reference.

With respect to the refresh timing circuit, claim 3 recites:

> The computer system of claim 2, wherein the refresh timing circuit further comprises:
> a clock generator for generating the clock pulses;
> a first counter coupled to the clock generator;
> a storage register coupled to the clock generator and the counter; and
> a comparator coupled to the clock generator, the counter and the storage register.

Claim 16 recites:

> The memory controller of claim 16, wherein the refresh timing circuit further comprises:
> a clock generator for generating the clock pulses;
> a first counter coupled to the clock generator;
> a storage register coupled to the clock generator and the counter; and
> a comparator coupled to the clock generator, the counter and the storage register.

Claim 38 recites:

> A refresh timing circuit comprising:
> an internal clock generator;
> a first counter coupled to the clock generator;
> a storage register coupled to the clock generator and the counter; and
> a comparator coupled to the clock generator, the counter and the storage register.

Appellant submits that nowhere in *The Rambus Disclosure* is there disclosed a refresh timing circuit having an internal clock generator, a counter, storage register or comparator. Accordingly, Claim Group II is patentable over *The Rambus Disclosure*.

For the foregoing reasons, Appellant submits that the Examiner has failed to search and find a printed publication or patent that discloses the claimed invention as set forth in MPEP § 706.02(a).

Claims 4-14 depend from claim 3, claims 18-27 depend from claim 17 and claims 39-49 depend from claim 38. Given that dependent claims necessarily include the limitations of the claims from which they depend, Appellant submits that the invention as claimed in claims 4-14, 18-27 and 39-49 are similarly not anticipated by *The Rambus Disclosure*.

Thus, the Examiner erred in rejecting claims 3-14, 17-27 and 38-49 under U.S.C. § 102(b).

IX. CONCLUSION

Careful review of the Examiner's rejections shows that the Examiner has failed to provide any reference, or combination of references of the prior art that shows all of the elements of each appealed claim. Therefore, Appellant respectfully submits that all appealed claims in this application are patentable and were improperly rejected by the Examiner during prosecution before the United States Patent and Trademark Office. Appellant respectfully requests that the Board of Patent Appeals and Interferences overrule the Examiner and direct allowance of the rejected claims.

This brief is submitted in triplicate, along with a check for $320.00 to cover the appeal fee for one other than a small entity as specified in 37 C.F.R. § 1.17(c). Please charge any shortages and credit any overcharges to our Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: 10/7, 2002

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X. APPENDIX OF CLAIMS (37 C.F.R. § 1.192(c)(9))

The claims on appeal read as follows:

1. A computer system comprising:

a memory; and

a memory controller, wherein the memory controller includes a refresh timing circuit for generating clock pulses used to trigger memory refresh events.

2. The computer system of claim 1, wherein the refresh timing circuit triggers memory refresh events whenever the computer system is operating in a normal mode and a low power mode.

3. The computer system of claim 2, wherein the refresh timing circuit further comprises:

a clock generator for generating the clock pulses;

a first counter coupled to the clock generator;

a storage register coupled to the clock generator and the counter; and

a comparator coupled to the clock generator, the counter and the storage register.

4. The computer system of claim 3, wherein the first counter counts the number of clock pulses generated by the clock generator.

5. The computer system of claim 4, wherein the first counter transmits data to the storage register whenever the computer system is operating in the normal mode, the data representing the number of clock pulses counted by the counter since the occurrence of a prior memory refresh event.

6. The computer system of claim 5, wherein the storage register transmits the data to the comparator upon a transition from the normal mode to the low power mode.

7. The computer system of claim 6, wherein the first counter transmits signals to the comparator whenever the computer system is operating in the low power mode, the signal representing the number of clock pulses received from the clock generator.

8. The computer system of claim 7, wherein the comparator compares the signal received from the first counter and the data received from the storage register, and wherein the comparator transmits a refresh trigger signal whenever there is a match between the signal and the data.

9. The computer system of claim 4, wherein the refresh timing circuit further comprises a second counter.

10. The computer system of claim 9, wherein the first counter counts the number of clock pulses generated by the clock generator while the computer system is operating in the low power mode and the second counter counts the number of clock pulses generated by the clock generator while the computer system is operating in a normal mode.

11. The computer system of claim 10, wherein the second counter transmits data to the storage register upon the occurrence of a memory refresh event whenever the computer system is operating in the normal mode, the data representing the number of clock pulses counted by the counter since the occurrence of a previous memory refresh event.

12. The computer system of claim 11, wherein the second counter is deactivated and the first counter is activated whenever the computer system transitions from the normal mode to the low power mode.

13. The computer system of claim 12, wherein the first counter transmits signals to the comparator whenever the computer system is operating in the low power mode, the signal representing the number of clock pulses received from the clock generator.

14. The computer system of claim 3, wherein the refresh timing circuit includes a second counter for triggering memory refresh events whenever the computer system is operating in the normal mode

15. The computer system of claim 1, wherein the memory is an Extended Data Out Dynamic Random Access Memory (EDO DRAM) and the memory controller is an EDO DRAM controller.

16. A memory controller comprising:

a refresh timing circuit for generating clock pulses used to trigger memory refresh events.

17. The memory controller of claim 16, wherein the refresh timing circuit further comprises:

a clock generator;

a first counter coupled to the clock generator;

a storage register coupled to the clock generator and the counter; and

a comparator coupled to the clock generator, the counter and the storage register.

18. The memory controller of claim 17, wherein the memory controller operates in a normal mode and a low power mode.

19. The memory controller of claim 18, wherein the first counter counts the number of clock pulses generated by the clock generator.

20. The memory controller of claim 19, wherein the first counter transmits data to the storage register whenever the memory controller is operating in the normal mode, the data representing the number of clock pulses counted by the counter since the occurrence of a previous memory refresh event.

21. The memory controller of claim 20, wherein the storage register transmits the data to the comparator upon a transition from the normal mode to the low power mode.

22. The memory controller of claim 21, wherein the first counter transmits signals to the comparator whenever the memory controller is operating in the low power mode, the signal representing the number of clock pulses received from the clock generator.

23. The memory controller of claim 22, wherein the comparator compares the signal received from the first counter and the data received from the storage register, and wherein the comparator transmits a refresh trigger signal whenever there is a match between the signal and the data.

24. The memory controller of claim 19, wherein the refresh timing circuit further comprises a second counter.

25. The memory controller of claim 24, wherein the first counter counts the number of clock pulses generated by the clock generator while the memory controller is operating in the low power mode and the second counter counts the number of clock pulses generated by the clock generator while the memory controller is operating in the normal mode.

26. The memory controller of claim 25, wherein the second counter transmits data to the storage register upon the occurrence of a memory refresh event whenever the memory controller is operating in the normal mode, the data representing the number of clock pulses counted by the counter since the occurrence of a previous memory refresh event.

27. The memory controller of claim 26, wherein the second counter is deactivated and the first counter is activated whenever the memory controller transitions from the normal mode to the low power mode.

28. The memory controller of claim 27, wherein the first counter transmits signals to the comparator whenever the memory controller is operating in the low power mode, the signal representing the number of clock pulses received from the clock generator.

38. A refresh timing circuit comprising:

an internal clock generator;

a first counter coupled to the clock generator;

a storage register coupled to the clock generator and the counter; and

a comparator coupled to the clock generator, the counter and the storage register.

39. The refresh timing circuit of claim 38, wherein the refresh timing circuit operates in a normal mode and a low power mode.

40. The refresh timing circuit of claim 39, wherein the first counter counts the number of clock pulses generated by the clock generator.

41. The refresh timing circuit of claim 40, wherein the first counter transmits data to the storage register whenever the refresh timing circuit is operating in the normal mode, the data representing the number of clock pulses counted by the counter since the occurrence of a previous memory refresh event.

42. The refresh timing circuit of claim 41, wherein the storage register transmits the data to the comparator upon a transition from the normal mode to the low power mode.

43. The refresh timing circuit of claim 42, wherein the first counter transmits signals to the comparator whenever the refresh timing circuit is operating in the low power mode, the signal representing the number of clock pulses received from the clock generator.

44. The refresh timing circuit of claim 43, wherein the comparator compares the signal received from the first counter and the data received from the storage register, and wherein the comparator transmits a refresh trigger signal whenever there is a match between the signal and the data.

45. The refresh timing circuit of claim 40, further comprising a second counter.

46. The refresh timing circuit of claim 45, wherein the first counter counts the number of clock pulses generated by the clock generator while the refresh timing circuit is

operating in the low power mode and the second counter counts the number of clock pulses generated by the clock generator while the refresh timing circuit is operating in the normal mode.

47. The refresh timing circuit of claim 46, wherein the second counter transmits data to the storage register upon the occurrence of a memory refresh event whenever the refresh timing circuit is operating in the normal mode, the data representing the number of clock pulses counted by the counter since the occurrence of a previous memory refresh event.

48. The refresh timing circuit of claim 47, wherein the second counter is deactivated and the first counter is activated whenever the refresh timing circuit transitions from the normal mode to the low power mode.

49. The refresh timing circuit of claim 48, wherein the first counter transmits signals to the comparator whenever the refresh timing circuit is operating in the low power mode, the signal representing the number of clock pulses received from the clock generator.